ABSTRACT

A planar transistor structure is disclosed that minimizes resistance in the source region and simplifies fabrication of the semiconductor device. The device includes a row of transistors where each transistor includes a stack gate structure and a drain, and a layer of type-2 polysilicon is used to interconnect the transistors in each row. A source region is provided adjacent to the layer of type-2 polysilicon that includes a contact and a N-type junction extending across the source region that provides a planar electrical path between the drains of the transistors and the contact, thereby reducing resistance of the source region.